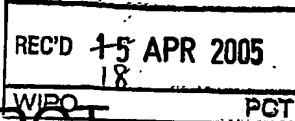


# PATENT COOPERATION TREATY

From the  
INTERNATIONAL SEARCHING AUTHORITY



To:

see form PCT/ISA/220

## WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY (PCT Rule 43bis.1)

Date of mailing  
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference  
see form PCT/ISA/220

**FOR FURTHER ACTION**  
See paragraph 2 below

International application No.  
PCT/JP2004/016082

International filing date (day/month/year)  
22.10.2004

Priority date (day/month/year)  
26.12.2003

International Patent Classification (IPC) or both national classification and IPC  
G11C11/56, G11C11/34, H01L45/00

Applicant  
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☒ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☒ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☒ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

### 2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA"). However, this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of three months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:



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**WRITTEN OPINION OF THE  
INTERNATIONAL SEARCHING AUTHORITY**

International application No.  
PCT/JP2004/016082

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**Box No. I Basis of the opinion**

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1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.
  - ☐ This opinion has been established on the basis of a translation from the original language into the following language , which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).
2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:
  - a. type of material:
    - ☐ a sequence listing
    - ☐ table(s) related to the sequence listing
  - b. format of material:
    - ☐ in written format
    - ☐ in computer readable form
  - c. time of filing/furnishing:
    - ☐ contained in the international application as filed.
    - ☐ filed together with the international application in computer readable form.
    - ☐ furnished subsequently to this Authority for the purposes of search.
3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
4. Additional comments:

**WRITTEN OPINION OF THE  
INTERNATIONAL SEARCHING AUTHORITY**

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**Box No. II Priority**

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1. ☐ The following document has not been furnished:

- ☐ copy of the earlier application whose priority has been claimed (Rule 43bis.1 and 66.7(a)).
- ☐ translation of the earlier application whose priority has been claimed (Rule 43bis.1 and 66.7(b)).

Consequently it has not been possible to consider the validity of the priority claim. This opinion has nevertheless been established on the assumption that the relevant date is the claimed priority date.

2. ☐ This opinion has been established as if no priority had been claimed due to the fact that the priority claim has been found invalid (Rules 43bis.1 and 64.1). Thus for the purposes of this opinion, the international filing date indicated above is considered to be the relevant date.

3. ☒ The International Searching Authority has not been able to consider the validity of the priority claim because a copy of the earlier application whose priority has been claimed was not available to the International Searching Authority at the time that the search was conducted (Rule 17.1). This opinion has nevertheless been established on the assumption that the relevant date is the claimed priority date.

4. Additional observations, if necessary:

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**Box No. IV Lack of unity of invention**

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1. ☒ In response to the invitation (Form PCT/ISA/206) to pay additional fees, the applicant has:

- ☒ paid additional fees.
- ☐ paid additional fees under protest.
- ☐ not paid additional fees.

2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose not to invite the applicant to pay additional fees.

3. This Authority considers that the requirement of unity of invention in accordance with Rule 13.1, 13.2 and 13.3 is

- ☐ complied with
- ☒ not complied with for the following reasons:

**see separate sheet**

4. Consequently, this report has been established in respect of the following parts of the international application:

- ☒ all parts.
- ☐ the parts relating to claims Nos.

**WRITTEN OPINION OF THE  
INTERNATIONAL SEARCHING AUTHORITY**

International application No.  
PCT/JP2004/016082

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**Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or  
Industrial applicability; citations and explanations supporting such statement**

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**1. Statement**

Novelty (N)	Yes: Claims	2-11,21-26,28-38
	No: Claims	1,12-20,27,39
Inventive step (IS)	Yes: Claims	4,25,31,36
	No: Claims	1-3,5-20-24,26,27-30,32-35,37-39
Industrial applicability (IA)	Yes: Claims	1-39
	No: Claims	

**2. Citations and explanations**

**see separate sheet**

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**Box No. VI Certain documents cited**

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**1. Certain published documents (Rules 43bis.1 and 70.10)**

and /or

**2. Non-written disclosures (Rules 43bis.1 and 70.9)**

**see form 210**

**Re Item IV.**

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

- 1) claims 1-11,32-39: Multibit memory device;
- 2) claims 12-20: Memory device structure; and
- 3) claims 21-31: Memory circuit with fewer read/write errors

The International Searching Authority considers that the present application contains 3 inventions. This observation is based on the following reasoning:

Reference is made to the following document D1:

D1: ZHUANG W W ET AL: "Novel colossal magnetoresistive thin film nonvolatile resistance random access memory (RRAM)" INTERNATIONAL ELECTRON DEVICES MEETING 2002. IEDM. TECHNICAL DIGEST. SAN FRANCISCO, CA, DEC. 8 - 11, 2002, NEW YORK, NY : IEEE, US, 8 December 2002 (2002-12-08), pages 193-196, XP010626021 ISBN: 0-7803-7462-2.

Document D1 discloses (see memory array, figure 13, page 195, right hand column; the references in parentheses applying to this document) a memory device (a memory array) comprising a first variable resistor (first RRAM cell) connected between a first terminal (wordline GND) and a third terminal (bitline) having a resistance which changes in accordance with a polarity of a pulse voltage between the first terminal and the third terminal; and a second variable resistor (second RRAM cell) connected between the third terminal (same bitline) and a second terminal (wordline 0V) having a resistance which changes in a direction opposite to a direction of change of the first variable resistor in accordance with a polarity of a pulse voltage between the third terminal and the second terminal.

Hence all features of independent apparatus claim 1 are known from D1 and said claim thus lacks novelty.

Dependent claim 2 and independent claim 12 share the following features:

a memory device comprising a (first) resistor having a resistance which changes in accordance with a polarity of a pulse voltage applied thereto.

These features are however known from prior art document D1 (see page 193, left-hand column, paragraph 2).

The special technical feature STF in the sense of Rule 13(2) PCT of claim 2 is thus constituted by:

the resistance value of the first variable resistor and the resistance value of the second variable resistor change in accordance with a first potential applied to two of the first terminal, second terminal and the third terminal and a second potential different from the first potential applied to the other terminal of the first terminal, the second terminal and the third terminal.

The problem to be solved by this feature could be said to be the provision of a multibit memory device (see description page 2, lines 10-25 of the present application).

Similarly independent claims 12 and 21 share the following features:

a memory device comprising a plurality of memory cells, each memory cell comprising a transistor connected to a variable resistor (layer) whose resistance value changes in response to a pulse voltage applied thereto.

These features are however also known from prior art document D1 (see figure 4)

The special technical feature STF in the sense of Rule 13(2) PCT of claim 12 is thus constituted by: an insulating layer formed over said transistor, said variable resistor film formed over the insulating layer.

The problem to be solved by this feature could be said to be the provision of a highly integrated memory cell with an increased degree of miniaturization (see description page 3, lines 1-20 of the present application).

Similarly independent claim 21 and dependent claim 2 share the following features:

a memory device comprising a variable resistor connected between a first and a second terminal whose resistance value changes in response to a pulse voltage applied between said terminals.

These features are however also known from prior art document D1 (see page 193, left-hand column, paragraph 2).

The special technical feature STF in the sense of Rule 13(2) PCT of independent claim 21

is thus constituted by:

a first memory block connected between a first node and a second node; a first block selecting transistor connected in series with the first memory block between the first node and the second node; and a second memory block connected between an interconnect node and a third node, the interconnect node connecting the first memory block and the first block-selecting transistor to each other, wherein each of the first and second memory blocks includes a plurality of memory cells connected in series, and each of the plurality of memory cells including a transistor coupled in parallel with the variable resistor between the first and second terminal.

The problem to be solved by this feature could be said to be the provision of a memory circuit with fewer errors in recording and reproduction (see description page 3, line 21 - page 4, line 25 of the present application).

The above analysis shows that there are no special technical features in the claimed 3 inventions, which are common. These features are not corresponding either, because they solve different, non related problems. Since common or corresponding STF's between the different inventions are missing, a technical relationship involving those features cannot be present and the different inventions are thus not linked by a single general inventive concept.

Hence the present application does not meet the requirements of Unity of invention as defined in Rule 13(1) PCT.

**Re Item V.**

**FIRST INVENTION: CLAIMS 1-11, 32-39**

1. The following further document is referred to in this communication:

D2 : US 2003/038301 A1 (MOORE JOHN) 27 February 2003 (2003-02-27); and

2. The present application does not meet the requirements of Article 6 PCT because:

**2.1** The expression "a second variable resistor (resistance means) having a resistance which changes (for changing resistance) in a direction opposite to a direction of change of the first variable resistor (resistance means)" in independent claims 1 and 39 respectively is not clear enough.

**2.2** The relation between the first, second and third terminals and the first and second variable resistance means in independent claim 39 is not defined, thus making said claim unclear.

**2.3** The expressions "the first pulse voltage" and "the second pulse voltage" in claim 10 are undefined.

**2.3** Although claims 1 and 39 have been drafted as separate independent claims, they appear to relate effectively to the same subject-matter and to differ from each other only with regard to the definition of the subject-matter for which protection is sought and in respect of the terminology used for the features of that subject-matter. In particular they do not relate to a plurality of inter-related products, different uses of a product or apparatus or alternative solutions to a particular problem, where it is not appropriate to cover these alternatives by a single claim.

Moreover, lack of clarity of the claims as a whole arises, since said plurality of independent claims makes it difficult to determine the matter for which protection is sought, and places an undue burden on others seeking to establish the extent of the protection.

Said claims thus lack conciseness contrary to the requirements of Article 6 PCT.

### **3. INDEPENDENT APPARATUS CLAIM 1**

Furthermore, the above-mentioned lack of clarity notwithstanding, the subject-matter of independent apparatus claim 1 does not meet the criteria of Article 33(1) PCT:

Document D2 discloses (see paragraphs [0021] - [0027] and figure 7; the references in parentheses applying to this document) a memory device (dual cell common electrode programmable metallization (PCRAM) memory device), comprising:



a first variable resistor connected (118) between a first terminal (source/drain of transistor 118<sub>AT</sub>) and a third terminal (common anode 110) having a resistance which changes in accordance with a polarity of a pulse voltage between the first terminal and the third terminal; and

a second variable resistor (120) connected between the third terminal (110) and a second terminal (source/drain of transistor 120<sub>AT</sub>) having a resistance which changes in a direction opposite to a direction of change of the first variable resistor in accordance with a polarity of a pulse voltage between the third terminal and the second terminal (for programmable metallization cells, an increase or decrease of the memory cell resistance value depends on the polarity of the applied voltage to the two electrode terminals (anode, cathode) of the cell).

Thus, as far as it can be understood (see point 2 of the present communication), all features of independent apparatus claim 1 are already known from D2 and said claim thus lacks novelty (Article 33(2) PCT).

#### **4. INDEPENDENT APPARATUS CLAIM 39**

Since the subject-matter of independent claim 39 corresponds to the subject matter of independent claim 1, the same reasoning as given for claim 1 will apply *mutatis mutandis*. Therefore claim 39 also does not meet the requirements of the PCT in respect of novelty (Article 33(2) PCT).

#### **5. INDEPENDENT METHOD CLAIMS 32 and 37**

The present application does not meet the criteria of Article 33(1) PCT, because the subject matter of independent method claims 32 and 37 does not involve an inventive step in the sense of Article 33(3)PCT:

Independent method claims 32 and 37 claim a three terminal variable resistance memory cell writing/resetting method and reading method respectively, whereby different potential combinations are applied to the terminals of said memory cell. These methods are however equally applicable to the three terminal memory cell described in D2 with the same result and the proposed methods in independent claims 32 and 37 thus cannot be

considered as inventive (Article 33(3) PCT).

**6. DEPENDENT CLAIMS 2-3, 5-11, 33-35, 38**

Dependent claims 2-3, 5-11, 33-35, and 38 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty and/or inventive step (Article 33(2) and (3) PCT).

**7. DEPENDENT CLAIMS 4 and 36**

Presently it appears that the combination of the features of dependent claims 4 and 36 are neither known from, nor rendered obvious by, the available prior art. The reasons are that none of the cited prior art documents discloses nor suggests a memory cell comprising first and second variable resistance means arranged and biased as described in claims 4 or 36 thereby allowing multibit data storage.

**SECOND INVENTION: CLAIMS 12-20**

1. The following further document is referred to in this communication:

D3: US-B1-6 583 003 (HSU SHENG TENG ET AL) 24 June 2003 (2003-06-24)

**2. INDEPENDENT APPARATUS CLAIM 12**

The subject-matter of claim 12 is not new in the sense of Article 33(2) PCT, and therefore the criteria of Article 33(1) PCT are not met.

Document D3 discloses (see column 2, line 19 - column 4, line 54 and figure 11; the references in parentheses applying to this document) a memory device whose resistance changes in accordance with a pulse voltage applied thereto (a 1T1R resistive memory array), the device comprising:

a plurality of memory cells (10), each memory cell comprising:

a transistor formed on a semiconductor substrate (50) and having a source (62), a drain (64) and a gate (60);

an insulating layer (70) formed over the transistor;

a variable resistance layer (76) formed over the insulating layer; and

two electrodes (74,78) formed on the variable resistance layer, wherein at least one of the drain and the source of the transistor are electrically connected to the two electrodes (drain (64) is connected to electrodes (74) and (78))

Thus all features of independent apparatus claim 12 are already known from D3 and said claim thus lacks novelty (Article 33(2) PCT).

### **3. DEPENDENT CLAIMS 13-20**

Dependent claims 13-20 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty and/or inventive step (Article 33(2) and (3) PCT) (see documents cited in search report)

### **THIRD INVENTION: CLAIMS 21-31**

1. The following further document is referred to in this communication:

- D4: WO-A2-02 19337 (MOTOROLA INC.) 07 MARCH 2002 (2002-03-07);
- D5: US-B1-6 226 197 (NAOKI NISHIMURA) 01 MAY 2001 (2001-05-01);
- D6: US-A-5 969990 (KENSHIRO ARASE) 19 OCTOBER 1999 (1999-10-19).

### **2. INDEPENDENT APPARATUS CLAIM 21**

The subject-matter of claim 21 does not meet the criteria of Article 33(1) PCT, because it does not involve an inventive step in the sense of Article 33(3) PCT.

Document D4, which is considered to represent the closest prior art document, discloses (see page 7, line 26 - page 9, line 14 and figure 3; the references in parentheses applying to this document)

a memory circuit (magnetic tunnel junction random access memory 15) comprising:

a first memory block (16) connected between a first node (ground connection of block 16) and a second node (19);

a first block-selecting transistor (28) connected in series with the first memory block between the first node and the second node; and

a second memory block (17) connected between the second node (19) and a third node (ground connection of block 17);

wherein each of the first and second memory blocks includes a plurality of memory cells (18) connected in series, and

each of the plurality of memory cells includes

a variable resistor (magnetic tunnel junction 26) connected between a first terminal and a second terminal and whose resistance value changes in response to a pulse voltage applied between the first terminal and the second terminal, and

a transistor (27) connected in parallel with the variable resistor (magnetic tunnel junction 26) between the first terminal and the second terminal.

**The subject-matter of claim 21 therefore differs from D4 in that said second memory block is connected between an interconnect node and a third node, the interconnect node connecting the first memory block and the first block-selecting transistor to each other (whereas in D4 a second block-selecting transistor is coupled between the second memory block and the second node (19)).**

The problem to be solved by the present invention may therefore be regarded as the provision of a low disturb memory device using a reduced chip area.

A memory circuit wherein more than one memory block is connected through a block-selecting transistor is however known from D6 (see memory blocks NAND1a and NAND2a connected by block-selecting transistor TG1a to bitline MBLa in figure 2) and the skilled person, without the exercise of inventive skill, would thus consider to connect said second memory block at said interconnect node, in order to solve the problem posed.

Hence claim 21 cannot be considered to involve an inventive step.

### **3. INDEPENDENT APPARATUS CLAIM 27**

The subject-matter of claim 27 is not new in the sense of Article 33(2) PCT, and therefore the criteria of Article 33(1) PCT are not met.

Document D4 discloses (see page 7, line 26 - page 9, line 14 and figure 3; the references in parentheses applying to this document)

a memory circuit (magnetic tunnel junction random access memory 15) comprising:

a first memory block (16) connected between a first node (ground connection of block 16) and a second node (19);

a first block-selecting transistor (28) connected in series with the first memory block between the first node and the second node;

a second memory block (17) connected between the second node (19) and a third node (ground connection of block 17);

a second block-selecting transistor (28) connected in series with the second memory block between the second node and the third node,

wherein each of the first and second memory blocks includes a plurality of memory cells (18) connected in series, and

each of the plurality of memory cells includes

a variable resistor (magnetic tunnel junction 26) connected between a first terminal and a second terminal and whose resistance value changes in response to a pulse voltage applied between the first terminal and the second terminal, and

a transistor (27) connected in parallel with the variable resistor (magnetic tunnel junction 26) between the first terminal and the second terminal.

Thus all features of independent apparatus claim 27 are already known from D4 and said claim thus lacks novelty (Article 33(2) PCT).

#### **4. DEPENDENT CLAIMS 22-24, 26, 28-30**

Dependent claims 22-24, 26 and 28-30 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty and/or inventive step (Article 33(2) and (3) PCT) (see documents cited in search report, especially D5, column 10, line 40 - column 11, line 18 and figures 15 and 16).

#### **5. DEPENDENT CLAIMS 25 and 31**

It appears that the subject-matter of dependent claims 25 and 31 fulfills the requirements of Article 33(1) PCT, because none of the cited prior art documents discloses nor suggests a reading method for a memory circuit according to claims 25 or 31 wherein voltages are applied between different memory blocks.

6. Some of the features in dependent apparatus claims 22-25 and 28-31 relate to a method for reading and writing a memory device rather than clearly defining the memory in terms of its technical features. The intended limitations are therefore not clear from these claim, contrary to the requirements of Article 6 PCT.

**WRITTEN OPINION OF THE  
INTERNATIONAL SEARCHING  
AUTHORITY (SEPARATE SHEET)**

International application No.

**PCT/JP2004/016082**

**Re Item VI**

**Certain documents cited**

**Certain published documents**

Application No Patent No	Publication date (day/month/year)	Filing date (day/month/year)	Priority date (valid claim) (day/month/year)
EP 1 426 966 A2	09.06.2004	04.12.2003	05.12.2002
EP 1 455 363 A1	08.09.2004	03.03.2004	06.03.2003